1.5 JOINT RESEARCH ACTIVITIES

1.5.1 JRA1- DETNI

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Observers: BNL

Project objectives

With the advent of pulsed spallation neutron sources driven by proton accelerators with multi-megawatt average beam power, as e.g. in the planned European Spallation Source ESS, the peak counting rates in the detectors will rise by up to two orders of magnitude in comparison with the presently strongest European neutron sources ILL and ISIS. Then, e.g. for novel applications like wavelength-resolved radiography, up to 10^8 neutrons/s (n/s) must be measured per detector module with two-dimensional spatial resolution of 50-100 µm and with 2 ns time resolution; at the huge counting rate the latter is necessary for unambiguous correlation of hits of the same event in the x and y detection planes with low chance coincidence rate. In addition, the full train of neutron wavelengths contained in each neutron beam pulse is resolved by time-of-flight measurements. For such most demanding applications, e.g. at ESS, in the JRA DETNI (DETectors for Neutron Instrumentation) prototypes of three novel single event counting neutron area detector types were developed together with the novel high-rate and high-resolution electronics for their operation. Whereas two of the prototypes are micro-strip detectors developed for 10^8 n/s rate and 50-100 µm spatial resolution capability, the third detector type is somewhat simpler and was built for rates of 10^7 n/s and 1 mm spatial resolution.

Methods

Current thermal neutron area detectors with gaseous converters limit the counting rate and spatial resolution capabilities to about 1 Mevent/s and 1 mm, respectively. Therefore, all three DETNI detector types contain, in combination with fast, high resolution two-dimensional position-sensitive detectors for the secondary radiation, few µm thick solid converter layers, which capture the neutron and emit promptly at least one quantum of detectable secondary radiation. In both micro-strip detector types ^{157}Gd converter layers are used in the central detector plane which emit for each captured neutron with 87% probability at least one fast (29-182 keV) conversion electron in random direction and which are thus sandwiched between two two-dimensional position-sensitive detectors for achieving maximal detection efficiency.

The first micro-strip detector type contains in each module four segments comprising each either side of the converter double-sided silicon micro-strip detectors of 53.3 x 53.3 mm^2 outer sizes with 640 micro-strips of 80 µm pitch in each of their two x and two y detection planes. The strips of each plane are read out via five novel 128-channel ‘n-XYTER’ ASIC (Application Specific Integrated Circuit) chips developed in DETNI, which are connected to a powerful multi-ADC-FPGA (Analogue Digital Converter - Field Programmable Gate Array) board. N-XYTER contains in each channel in parallel a fast trigger circuit with novel amplitude time walk compensation and a slow amplitude (energy) signal circuit and gives out with 32 MHz in parallel via derandomizing digital and analogue pipelines and a token-ring based four-fold multiplexer, with additional built-in derandomization, sparsification and dynamic bandwidth distribution functions, for each hit the digitized strip coordinate, a 2 ns wide, 14 bit deep time stamp information and the corresponding analogue amplitude fraction deposited on the strip. Thus, by calculating for each event and in each detection plane the centre of gravity of the amplitude distribution on adjacent strips, the spatial resolution is improved versus digitized strip coordinate readout. In addition, background is suppressed by energy gating.

The second micro-strip detector type contains a central composite converter foil and on either side 4.5 mm deep three-stage low-pressure (20 mbar) gas avalanche multiplication gaps, which are closed by novel multilayer two-dimensional position-sensitive Micro-Strip Gas Chamber (MSGC) plates. The novel composite converters comprise either side of a Kevlar support foil ^{157}Gd converter layers coated with 1 µm thick columnar CsI secondary electron (SE) emitter layers. Thus, after neutron capture each fast conversion electron emits a detectable cluster of slow SEs from one of the converter sides into the adjacent gas volume. There the SEs are extracted from the structured converter and pre-amplified by means of 8-10 kV/cm electrical field strength applied over a depth of 250 µm between the converter and extraction grids mounted either side of the converter. The fraction of SEs scattered through the grid is further multiplied in the subsequent 3.75 mm deep constant field region, until the avalanche reaches the rising field region on the last 0.5 mm to the MSGC plate anodes where additional micro-strip amplification occurs. The MSGC plates were optimized for low-pressure operation by widening the high-field region between the anode and cathode micro-strips by field shaping to attain higher micro-strip amplification. In addition, through a controlled diffusion widening of the avalanche head, for each event hits are induced on 3.5 adjacent strips on average, thus giving optimal conditions for precise position calculation using the centre of gravity method. The MSGC detector is read out via the 32-channel 'MSGCROC' variant of the novel ASIC family developed in DETNI, which has variable amplification and a five times higher counting rate capability of 900 khit/s per micro-strip than n-XYTER (Fig. J1).

The third detector type called CASCADE contains in a pressure gas vessel, on either side of a central two-dimensional position-sensitive signal induction and readout electrode, stacks of up to five GEM (Gas Electron Multiplier) foils in 2 mm distance. The latter consist of insulating 50 µm thick Kapton foils with copper claddings on both sides, which are perforated by double-sided etching with a regular structure of holes of 70 µm diameters in 140 µm pitch. In addition, on either side of the GEM foils 1 µm thick ^{10}B neutron converter layers are deposited, which emit promptly ^{7}Li and α ions in the 1-MeV range after neutron capture. The latter release along their tracks during their stopping secondary electrons in the gas volume, which are drifted without gas amplification through the GEM holes towards the central readout electrode. Only when passing through the last GEM foil they are sufficiently amplified for detection by applying higher field strength. For readout again the n-XYTER ASIC is used which is optimized for low-charge signals.

Impact

The novel detector and readout electronics technology, which were developed and prototyped in DETNI, proves the capability of these innovations to advance thermal neutron detection from the 1 Mevent/s counting rate and 1 mm spatial resolution level to the 100 Mevent/s and 50-100 µm level, with single event counting, fast timing and neutron wavelength resolution, as needed for coping with demanding applications at next generation spallation neutron sources.

The unique channel-wise triggered ASIC chips developed in DETNI for high-rate micro-strip readout are in addition used as prototypes at high-energy heavy-ion detectors for FAIR/GSI and as basis for developing there a dedicated radiation hard version. The DETNI ASIC and readout board developments could also progress synchrotron and X-ray detection, and after adding variable shaping time functionality to the variable gain function in the MSGCROC ASIC, slower 'standard' thermal neutron and X-ray detector types like multi-wire chambers with single-wire readout.

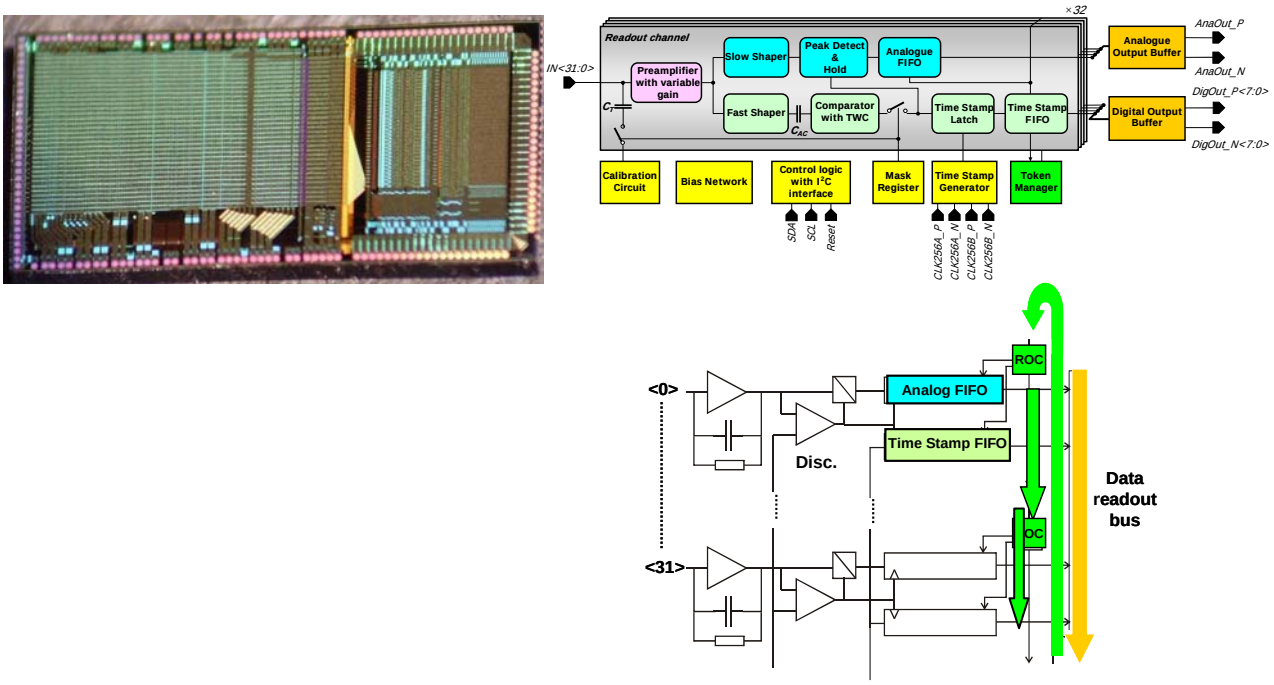

Figure J1**.** As an example of the work completed in DETNI this figure shows the 32-channel MSGCROC ASIC (top left) together with a block diagram of the ASIC architecture (top right) including the token-ring readout scheme used (bottom right). The variable gain preamplifier measures both signal polarities. By means of the fast-shaped signal circuit with comparator and time walk compensation (TWC) each ASIC channel is triggered individually, and 2 ns wide time stamps are stored in 14 bit depth, synchronized by two phase-shifted 250 or 256 MHz clocks. In the slow shaper with peak detect and hold circuit in addition an analogue (energy) signal is generated. Both, the digital signals (including e.g. also the channel addresses) and the analogue signals are buffered each in four FIFO cells deep pipelines for deramdomization. For readout the analogue and digital signals are given out coincident with 32 MHz per channel via the indicated token-ring scheme; thereby the 32 bit digital signals are four-fold multiplexed, i.e. read out in four 8-bit packages with 128 MHz each. The token-ring scheme includes further derandomization and sparsification (zero suppression), skipping empty channels and blocks of 16 empty channels.